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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,265	03/12/2004	Tyler Lowrey	2024.46	7228

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,265	LOWREY ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 7-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 7-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The cancellation of claims 2-6 in Paper filed on 4/1/05 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 7-9 and 12-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Harshfield (US. 6,031,287).

Regarding claims 1 and 12-13, Harshfield (Figs. 20-24) discloses a method of making an electrically programmable memory element, comprising: providing a first dielectric layer 110, the first dielectric layer 110 having a sidewall surface; forming a conductive sidewall spacer 124 over the sidewall surface; forming a second dielectric layer 122 over the conductive sidewall spacer 124; and forming a programmable

resistance material 130 of chalcogenide (column 14, lines 1-5) in electrical contact with a top surface of the conductive sidewall spacer 124.

Regarding claims 7-8 and 14-15, Harshfield (Fig. 24) further discloses that the programmable resistance material 130 of a chalcogenide material is a phase-change material (column 2, lines 27-36).

Regarding claim 9, the first dielectric layer 110 and the second dielectric layer 122 are formed of the same material (column 13, lines 45-47).

4. Claims 1, 7-9 and 12-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Gonzalez et al (US. 5,854,102).

Regarding claims 1 and 12-13, Gonzalez (Figs. 29-30) discloses a method of making an electrically programmable memory element comprising: providing a first dielectric layer 156 (not labeled, see column 15, lines 4-7), the first dielectric layer 156 having a sidewall surface; forming a conductive sidewall spacer 160 (see Fig. 29) over the sidewall surface; forming a second dielectric layer 168 over the conductive sidewall spacer 160; and forming a programmable resistance material 164 of chalcogenide element (column 15, lines 45-50 and column 8, lines 30-40) in electrical contact with top surface of the conductive sidewall spacer 160.

Regarding claims 7-8 and 14-15, Gonzalez (Fig. 30) further discloses that the programmable resistance material 164 of a chalcogenide element is a phase-change material (column 3, lines 14-19).

Regarding claim 9, Gonzalez further discloses that the first dielectric layer 156 and the second dielectric layer 168 are formed of the same material (column 15, lines 54-55).

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 7-9, and 12-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Ovshinsky et al (US. 5,414,271).

Regarding claims 1 and 12-13, Ovshinsky (Fig. 1) discloses a method of making an electrically programmable memory element, comprising: providing a first dielectric layer 20, the first dielectric layer 20 having a sidewall surface; forming a conductive sidewall spacer (32,34) over the sidewall surface; forming a second dielectric layer 39 over the conductive sidewall spacer (32,34); and forming a programmable resistance material 36 of a chalcogenide element (column 16, lines 52-54) in electrical contact with a top surface of the conductive sidewall spacer (32,34).

Regarding claims 7-8 and 14-15, Ovshinsky (Fig. 1) further discloses that the programmable resistance material 36 of chalcogenide element is a phase-change material (column 9, lines 45-51).

Regarding claim 9, Ovshinsky further discloses that the first dielectric layer 20 made of silicon dioxide (column 16, lines 19-20), which is the same material as the second dielectric layer 39 of silicon dioxide (column 18, lines 30-33).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harshfield (US. 6,031,287).

Harshfield does not disclose an anisotropically etching being used to form the conductive sidewall spacer 124.

However, Harshfield further discloses that the forming conductive sidewall spacer 124 comprises conformally depositing the conductive material 118 over the dielectric material 110 (Fig. 20) and removing the portions of the conductive material 118 extending on the surface of the dielectric material 110 by an etching process (column 14, lines 56-60). Therefore, it would have been obvious to use an anisotropically etching to etch the conductive material 118 for forming the sidewall spacer 124 because as is well known, an anisotropically etching performs the vertical etching which is commonly used for removing any portions of the conductive material extending on the surface of the dielectric material.

9. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinsky et al (US. 5,414,271).

Ovshinsky does not disclose an anisotropically etching being used to form the conductive sidewall spacer (32,34).

However, Ovshinsky further discloses that the forming conductive sidewall spacer (32,34) comprises conformally depositing the conductive material over the dielectric material 20 and removing the portions of the conductive material extending on the surface of the dielectric material 20 by an etching process (column 18, lines 36-43). Therefore, it would have been obvious to use an anisotropically etching to etch the conductive material for forming the sidewall spacer (32,34) because as is well known, an anisotropically etching performs the vertical etching which is commonly used for removing any portions of the conductive material extending on the surface of the dielectric material.

Response to Arguments

10. Applicant argues that the conductive material 160 shown in Fig. 29 of Gonzalez and the conductive material (32,34) shown in Fig. 1 of Ovshinsky are not conductive sidewall spacers.

This argument is not persuasive. As is well known in the semiconductor arts, these conductive layers are defined as "conductive sidewall spacer" because they are formed along a sidewall surface of the opening. For example, the U.s. Patent No. 6,258,707 issued to Uzoh is cited to illustrate the use of term "conductive sidewall spacer". Specifically, Uzoh (Fig. 9) discloses a conductive sidewall spacer 124 (column 8, lines 62-67), which is defined as a conductive layer formed along a sidewall surface of he opening.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
June 10, 2005

PHAT X. CAO
PRIMARY EXAMINER